Virtex-II Pro PowerPC SEE Characterization Test Methods and Results

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Abstract

The Xilinx Virtex-II Pro is a platform FPGA that embeds multiple microprocessors within the fabric of a SRAM-based reprogrammable FPGA. The variety and quantity of resources provided by this family of devices make them very attractive for spaceflight applications. However, these devices will be susceptible to single event effects (SEE), which must be mitigated.

Observations from prior testing of the Xilinx Virtex-II Pro suggest that the PowerPC core has significant vulnerability to SEEs. However, these initial tests were not designed to exclusively target the functionality of the PowerPC, therefore making it difficult to distinguish processor upsets from fabric upsets. The main focus of this paper involves detailed SEE testing of the embedded PowerPC core. Due to the complexity of the PowerPC, various custom test applications, both static and dynamic, will be designed to isolate each unit of the processor. Collective analysis of the test results will provide insight into the exact upset mechanisms of the PowerPC. With this information, mitigations schemes can be developed and tested that address the specific susceptibilities of these devices.

I. INTRODUCTION

NASA/GSFC has been involved with testing the Xilinx Virtex-II Pro devices. Initial heavy-ion radiation tests were performed using commercial-grade devices on COTS boards [1, 2]. During these tests, no destructive single event latchup (SEL) event was observed to a LET of 53.9 MeV-cm^2/mg and a fluence of 10^7 ions/cm^2. However, these tests have suggested that the embedded PowerPC processor is prone to many SEEs in a radiation environment.

The objective of this test is to focus on the SEEs that occur within the embedded PowerPC of the Virtex-II Pro FPGA family. The test applications will be designed to isolate the main units of the PowerPC (i.e. registers, cache, execution unit). The goal of this test is to produce results that will provide a detailed understanding of where upsets can occur and how they affect PowerPC operation. With this knowledge, system and device-level mitigation schemes can be developed that address each upset mechanism.

This test will be performed on multiple XQR2VP40 devices, a dual processor version of the Virtex-II Pro with an epitaxial layer that helps reduce radiation effects. This device includes 15.9 million configuration bits, 3.4 Mb of BlockRAM, 12 RocketIO^{TM} Multi-Gigabit Transceivers (MGT), 8 Digital Clock Managers (DCM), and 192 dedicated 18x18 multipliers [3]. The XQR2VP40 device will be tested using the Xilinx Radiation Test Consortium (XRTC) board specifically designed for radiation testing of the Virtex-II Pro.

This test will be conducted at the Indiana University Cyclotron Facility (IUCF) in Bloomington, Indiana. This facility is capable of producing protons with a LET range of 30 to 200 MeV and a flux of 1E2 to 1E11 p/sec-cm^2 [4].

II. TEST DETAILS

A) Instrumentation

The test instrumentation is illustrated in Figure 1. One laptop with a PCMCIA GPIB card serves to control the power supplies (Agilent 6623 and 6624) and record the voltage and currents for each DUT and motherboard power rail in strip-chart form using existing software [5]. GPIB extenders are used between the test chamber and user area. A second laptop is used to record all serial data received from the FuncMon UART. A third laptop is used for programming the DUT via JTAG. DUT PowerPC information is also transmitted over this link upon request of the user. Due to incompatible software/firmware with the existing JPL counter boards, custom LED/Switch boxes, pictured in Figure 2, are used to provide control/status to the FuncMon and ConfigMon FPGAs on the SEAKR motherboard. This

problem is discussed further in the Test Complications section. The cable distance from the beam-line to the user area is approximately 60 feet. Custom high-speed LVDS driver/receiver cards, pictured in Figure 3, are used to move data between the test chamber and user area over 40-pin twisted-pair ribbon cables. Figures 4, 5, and 6 show the board mounted vertically in the beam-line.
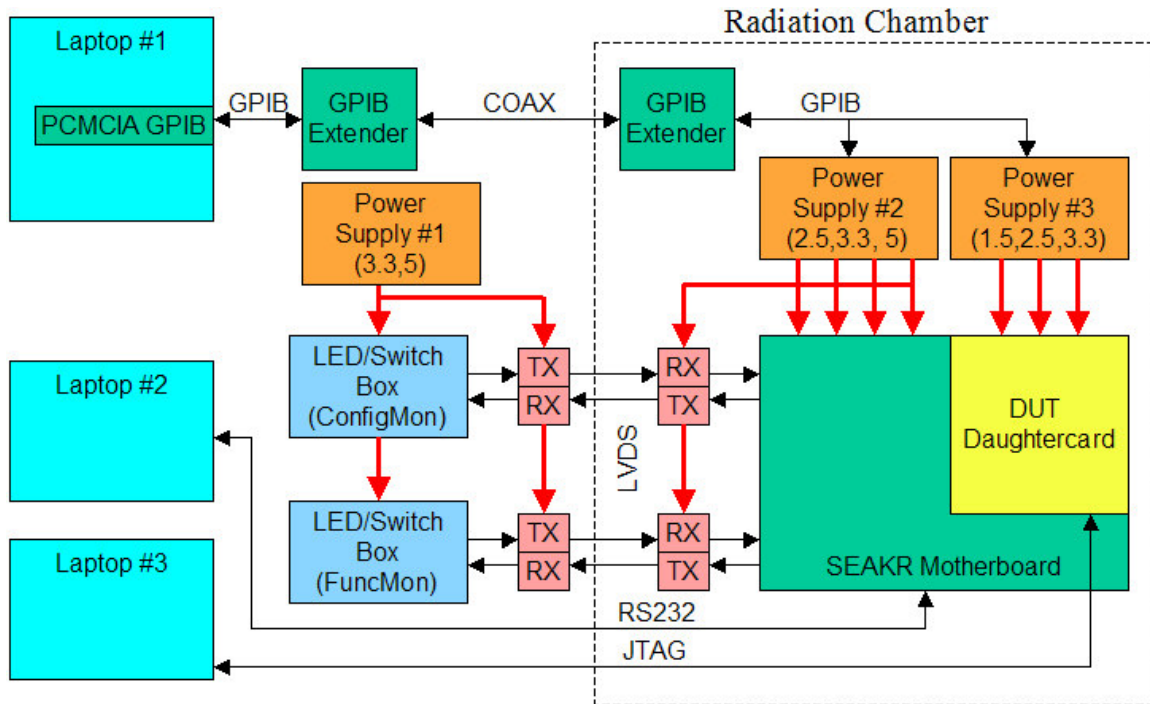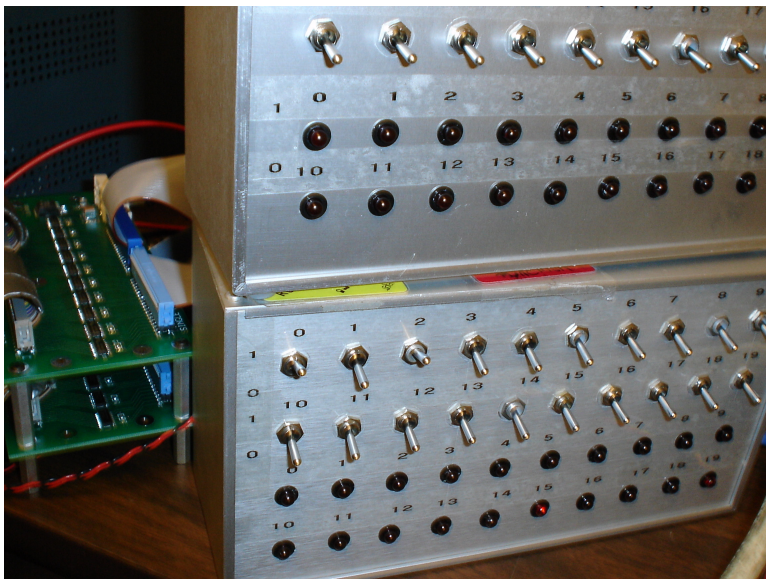

Figure 1 – Test Setup
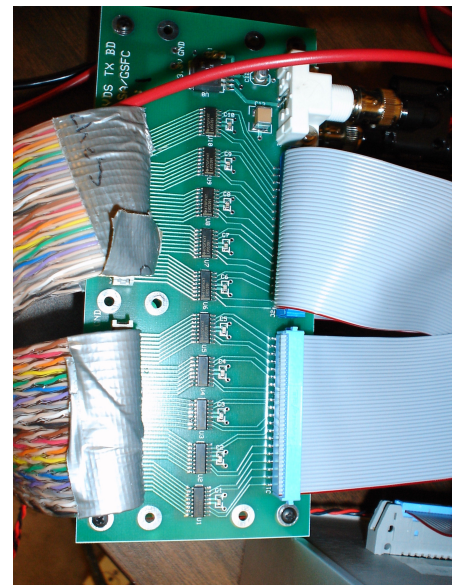

Figure 2 – FPGA LED/Switch Boxes
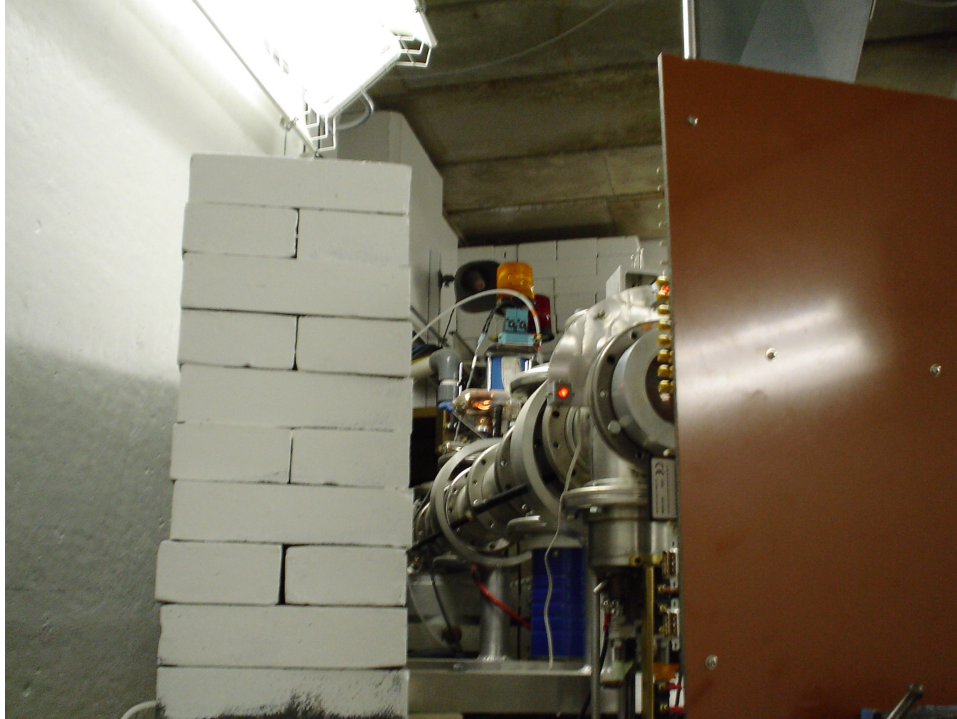

Figure 3 – LVDS Driver/Receiver Cards

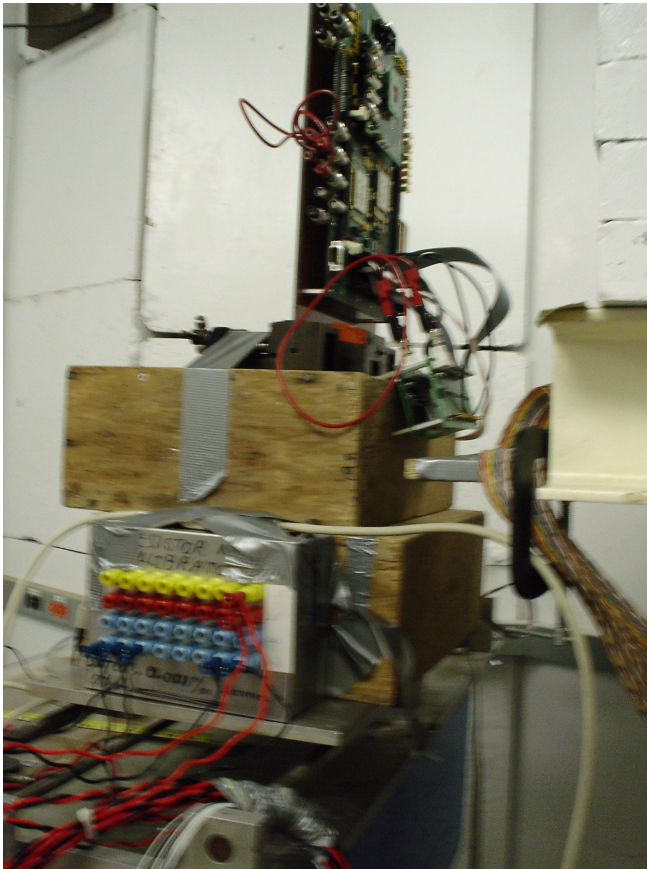Figure 4 – XRTC V2Pro Board at IUCF Proton Beam

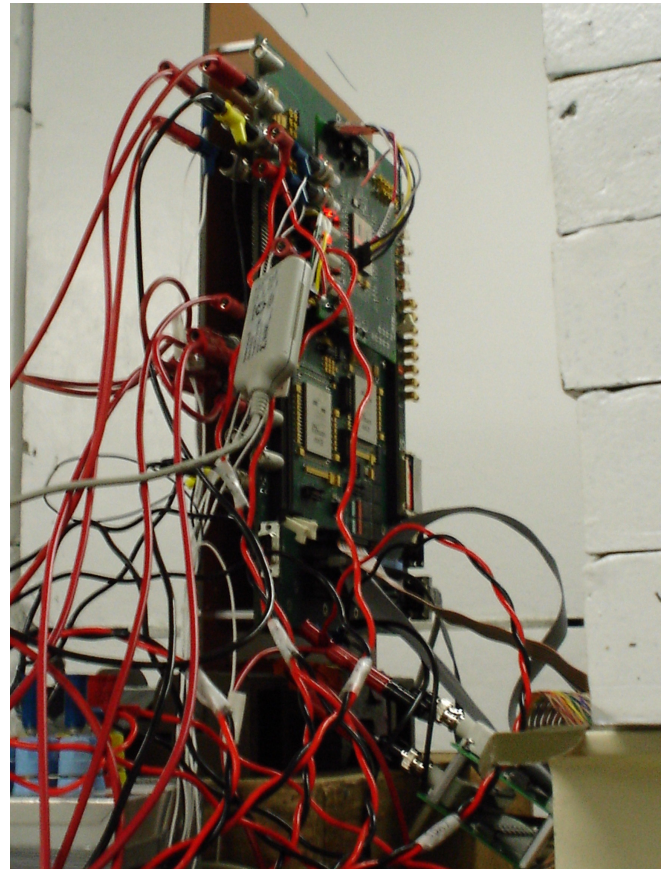Figure 5 – XRTC Board without Cabling

Figure 6 – XRTC V2Pro Board with Cabling

B) Test Complications

(1) DUT Socket

A few critical problems were faced during this radiation test. The biggest issue was the socketed DUT card. There were many faulty connections between the FPGAs and the 1152-pin spring-loaded socket pictured in Figure 7. This was determined using an I/O test program to exercise all single-ended I/Os available between the FuncMon and DUT FPGAs. When swapping DUT FPGAs, the location of working lines changed, requiring a modification in the DUT constraint file (*.ucf). In addition, tightening or loosing any of the eight screws also seemed to have an effect on the signals that worked properly. For example, a quarter turn on one of the screws caused an additional signal to work, but a quarter turn on a different screw caused another signal to fail.
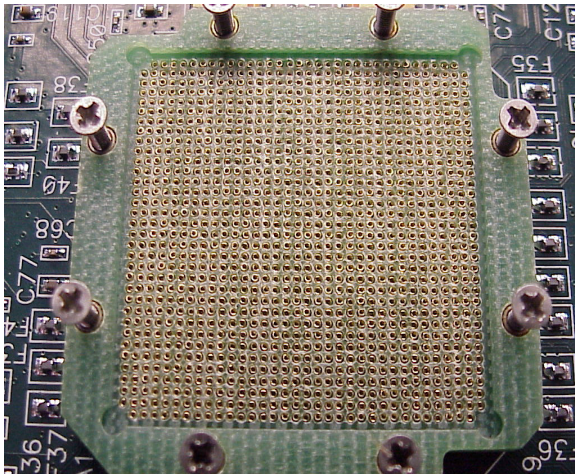

Figure 7 – FPGA Socket

After the test, the socket was inspected with a stereomicroscope. We found that a large number of the connection springs were not aligned properly. Some were below the surface of the socket, some were above, and a lot of the springs were angled in different directions.

Problems also existed with the JTAG connection on the socketed DUT card; therefore we were only able to run one of two tests using this card that did not require PowerPC access via JTAG. We were able to run both tests using another DUT card with a soldered FPGA.

(2) Configuration Scrubbing

In order to isolate SEEs within a device, scrubbing the DUT configuration bitstream is required for radiation testing [6, 7, 8]. We were unsuccessful in getting the ConfigMon FPGA to configure and scrub the DUT configuration bitstream. We used the SelectMAP controller design provided by Xilinx, which we controlled and monitored using the 40-pin IDE connectors on the SEAKR motherboard.

The DUT .bit and .msk files were properly loaded into the configuration and mask PROMs, respectively. The DUT programming mode pins (SW16 on SEAKR board) were set for Master SelectMAP. All significant control lines on the ConfigMon FPGA (configure_dut, rdbk_dut, scrub_dut, rst_cfg) were held low. To configure the DUT, configure_dut was pulsed high. Following, the configure_finish status signal would constantly blink as if the configuration core was continuously trying to configure the DUT. Also, the sefi_error status signal would stay high. The rst_cfg would successfully reset the configuration core, turning off the configure_finish and sefi_error status signals.

(3) Counter Boards

The JPL counter boards are meant to control the communication between the SEAKR motherboard FPGAs with laptops that are populated with digital I/O cards. In order for these to work properly, the software on the laptops, VHDL on the counter board FPGA, and VHDL on the SEAKR FPGAs must interface correctly with each other. The problem that we had/have is that we have two newer versions of the counter boards, instead of an older wire-wrapped version which communicates with the ConfigMon FPGA. At the time of our test, the ConfigMon and counter board FPGA interfaces did not match. Xilinx and JPL are still in the process of upgrading the test system such that both FuncMon and ConfigMon FPGAs use identical versions of the counter board.

To run this test, the method of communication needed to be solved without the aid of the JPL counter boards. Due to time constraints, a more manual, but effective approach was taken to give the user control over critical control signals and the ability to monitor the status of the FPGAs. Two identical control boxes (Figure 2) were built, one for FuncMon and one for ConfigMon. The control box consists of 20 toggle switches, 20 LEDs, and two 40-pin ribbon connectors. The connectors were designed to match the SEAKR motherboard IDE connectors (odd pins grounded). The switch-side connector was cabled to the FuncMon/ConfigMon_In IDE connector on the SEAKR board. The FuncMon/ConfigMon_Out

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IDE connector on the SEAKR was cabled to the LED-side connector of the control box. The control box requires an input voltage of 3.3 volts.

C) Test Applications

The main goal of this proton radiation test was to collect data that would quantify the SEUs that occur within the PowerPC registers and cache units. Two test applications, one static and one pseudo-static, were used for this radiation test. The static test requires the ability to connect to the JTAG port of the PowerPC. However, due to the socket problems, this test could not be run using the socketed DUT card since connection to the PowerPC could not be made. The pseudo-static test does not require this functionality. Again, due to socket problems, this test was only run on one of three FPGAs using the socketed DUT card. Time did not allow for troubleshooting and reassigning each of the FPGAs faulty single-ended signals during beam time. Therefore, the pseudo-static test was only successful on one socketed FPGA. Both tests were run using the soldered DUT card. Note that for both tests, exception handlers were not implemented.

1) Static Test Application

This application uses the Xilinx Microprocessor Debugger (XMD) tool to read out the register and cache data at the end of each run through the Xilinx Parallel-III JTAG cable. Therefore, for this application to work properly, the PowerPC JTAG circuitry and routing cannot be corrupted by radiation. Before the device is irradiated, the DUT PowerPC initializes all of its general-purpose registers (GPR) to known values using a one-hot scheme. For example, GPR_0 is set to 0x0000_0001, GPR_1 is set to 0x0000_0002, GPR_2 is set to 0x0000_0004, and GPR_31 is set to 0x8000_0000. This way, each register has a unique value instead of initializing them to equal values (i.e. all 0's or 1's). The processor then enters an infinite loop. Then all D-cache values are set to 0x0000_0000, 0xFFFF_FFFF, or 0xAAAA_AAAA using the XMD tool. After irradiating the DUT, the XMD

tool is used again to dump all register and D-cache data for post-test analysis. From previous testing, it will not be difficult to detect a bad run due to a JTAG SEFI [1].

2) Pseudo-Static Test Application

The purpose of this test application is to gather statistical data on how often the registers experience SEUs. In addition to controlling DUT resets, the FuncMon design includes a custom DUT_Control_Unit hardware core that periodically sends an interrupt to the DUT PowerPC core (IRQ frequency of 1-Hz). Upon receiving the interrupt, the DUT PowerPC proceeds to dump all register data (GPRs and SPRs) to the FuncMon using a processor local bus (PLB) GPIO data link. The FuncMon receives the data and stores the register value in BRAM and increments a counter. This is considered a "pseudo-static" test design, rather than a dynamic test design, since the DUT PowerPC runs minimal code during a test (less than 1% duty-cycle). Halted or corrupted data streams will identify the possibility of an instruction set upset, mishandled processor exception, processor reset, or other TBD SEFI. In order to minimize this occurrence, the assembly instruction set for the DUT PowerPC will be made as small as possible. A block diagram for this design is depicted in Figure 8.

Once the data transfer is complete, the FuncMon PowerPC will receive an interrupt from the DUT_Control_Unit. The FuncMon PowerPC will then dump all recorded data to the UART port. Each data dump will be time-tagged. Logging the SPR data may provide insight as to how the PowerPC is affected by SEUs.

The clocking is derived using a DCM within the FuncMon FPGA. The ConfigMon FPGA supplies the FuncMon with a 33 MHz clock. The DCM performs a 2x and 4x operation, yielding two clock speeds of 66 MHz and 132 MHz. The DUT FPGA logic, DUT PowerPC, and FuncMon FPGA logic all operate at 66 MHz. The FuncMon PowerPC operates at 132 MHz.

Figure 8 – Dynamic PowerPC Test Block Diagram

III. RESULTS

A) Static Test Discussion

The static test was run on only the soldered DUT card. Of the nine runs, five were unsuccessful due to bad data at the end of the run. The data shows that all registers and data cache are set to either all 0's, all 1's, or 0x3C75. Table 1 shows the breakdown of these occurrences. In both cases of the SPR contents being set to 0x3C75, the program counter register (SPR PC) is the only one set to 0x3C71.

During the May Xilinx/JPL test at TAMU, similar observations were made when using the Agilent probe that was controlling the PowerPC JTAG port [9]. This could be the result of a PowerPC SEE (reset, instruction, exception, etc.). However, three out of nine runs (all three were bad runs), the DUT could not be reprogrammed via JTAG, requiring a power cycle. This suggests the possibility of a JTAG SEFI. The DUT did not require a power cycle when "good" data was extracted after irradiation. Other observations include activity on the PIT (3 runs), PC set to 0xFFFF_FFFC (PowerPC boot-loader address; 2 runs), and a total of six random bit errors within the SPRs.

Table 1: Static Test Failures

PowerPC Unit	All '0's	All '1's	All 0x3C75
GPRs	3	1	1
SPRs	2	1	2
D-Cache	2	1	2

Table 2 summarizes the data collected from the four good runs. All testing was done with a proton beam energy of 200 MeV. The flux for the static test was approximately 2.0E8 (p/s-cm^2).

Table 2: Static Reg/D-Cache Data

PowerPC Unit	Total Bit-Errors	Cross (cm^2)	StDev	Cross/bit (cm^2)	StDev
GPRs	4	4.99E-11	2.50E-11	4.88E-14	2.44E-14
D-Cache	87	4.34E-9	2.33E-10	3.31E-14	1.78E-15

B) Pseudo-Static Test Discussion

The pseudo-static test was run on the soldered DUT card and on one FPGA mounted in the socketed DUT card for a total of 24 runs. All testing was done with a proton beam energy of 200 MeV. The flux for the dynamic test ranged from 3.5E7 to 6.0E7 (p/s-cm^2). Each test was run until the DUT PowerPC stopped responding to interrupt requests (IRQ). These were recorded as a general PowerPC SEFI. There was no data that suggested what type of SEE was possibly occurring. Post-analysis of the data shows that no significant number of bit errors occurred within the PowerPC registers. On three separate runs, the PowerPC failed in the middle of the interrupt service routine (ISR) and did not respond to following IRQs.

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This facility is shared with cancer treatment patients. The radiation test is paused when the treatment center requires use of the radiation source. This occurred two times during dynamic testing. When the beam was turned back on, the DUT PowerPC immediately failed to respond to IRQs. There was another interesting observation. During one of the runs, the PowerPC started to respond only to every other IRQ. This lasted for 32 interrupt cycles, and then it failed to respond to any IRQs. Finally, the 32-bit GPIO bus was only hit during two runs. This was easy to tell due to "stuck-at" bits that were common in all recorded data values. The corruption of the GPIO bus does not cause the test application to fail. Table 3 shows the SEFI results of the pseudo-static test application. Two cross-section data points are computed. The first computes the cross-section based on the average of 24 separate cross-sections. The second computes the cross-section by treating all 24 runs as one run with 24 errors.

Table 3: Dynamic PowerPC SEFI Data

Computation Method	Cross (cm^2)	StDev
Average of 24 runs	9.54E-10	7.51E-10
One run with 24 errors	4.79E-10	9.77E-11

IV. CONCLUSIONS

We were successful in collecting static PowerPC register and cache data that appears to be reasonable even though exception handlers were not built into the code. The SEEs that we observed from the pseudo-static test application could be attributed to a number of different upset mechanisms. The DUT design was not triplicated or scrubbed. Therefore, the PowerPC "SEFIs" could simply be the result of an instruction upset or a configuration/routing bit upset associated with the PLB. Future testing is needed that integrates triplication and configuration scrubbing, including the BRAM scrubber core that Xilinx is currently testing [8]. The data collected from this round of testing is a good data point to compare to following these future tests, which will eliminate the effect of configuration/BRAM SEUs.

The DUT socket gave us numerous problems that essentially limited our testing to one FPGA. Unless these issues are solved, we will lean toward procuring additional soldered DUT cards. This will eliminate the hassle and uncertainty of reworking the designs every time the FPGAs are swapped. In addition to decreasing the amount of wasted beam time, it will increase the quality and quantity of the data collected.

V. ACKNOWLEDGEMENTS

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